II. Amendments to the Drawings

The Examiner has objected to the drawing as it would fail to show every feature of the invention as claimed. A replacement sheet including changes to Figure 1 is attached.

III. Remarks

Reconsideration and re-examination of this application in view of the above amendments and the following remarks is herein respectfully requested.

After entering this amendment, claims 1-7 and 9-17 remain pending.

Claim Objections

The Examiner has objected to claims 12 and 15 for having improper dependencies. Claim 12 has been amended to now dependant claim 1 because the subject matter of originally filed claim 8 has been inserted into previously amended claim 1. Claim 15 has been amended by reciting explicitly that the claimed device is set up to execute the method claimed in currently amended claim 1.

Claim Rejections – 35 U.S.C. § 101

Claims 16 and 17 were rejected under 35 U.S.C. § 101 because they fail to recite a useful, concrete and tangible result. Claims 16 and 17 have been amended to now recite explicitly the method of claim 1 that is to be executed by a computer program product or from a digital storage medium that has electronically readable control signals stored omit. Thus, the computer program product is a computer program is a product that is sold for use in the verification of digital circuits. The program may be sold on a digital storage medium. Therefore the digital storage medium and the computer program product result in a useful, concrete, and tangible result.

Claim Rejections - 35 U.S.C. § 112

Claims 13 and 15 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Regarding claim 13, the Examiner argues that "a method of equivalence class refinement" would not be defined in claims. Claim 13 has been amended to now recite that determining the implementation alternative is at least partially performed by a method of equivalence class refinement in order to comply with the enablement requirement.

With respect to claim 15, the Examiner argues that the claim would fail to describe how the person skilled in the art could use the device of claim 14 to execute the method of claim 1. Claim 15 has been redrafted to read now that the device is adapted to execute the method as recited in claim 1.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 4-6, 9-12, and 14-15 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,301,687, to Jain, et al. ("Jain"). Applicant respectfully traverses these rejections.

Jain relates to a method for the verification and analysis of digital circuit designs. The method of Jain verifies the functionality of a circuit design at different levels of the design cycle hierarchy against the design specification from the previous level (column 1, line 47 to 51). Thereby, each level results in a different description of the same design. The equivalence of new level is checked against a previously verified specification of the circuit. This check is

termed implementation verification in Jain. However, Jain states that a first description of the design of a digital circuit is verified against the original specification and if the verification is successful, the specification is replaced by this description as a new basis for further verification (column 1, lines 56 to 61). Thus, the different descriptions of the digital circuit are replaced successively by a further specified or developed description of the digital circuit. Jain uses the term implementation to identify the subsequent descriptions of the same digital circuit.

As to claim 1, the term implementation alternative utilized in the present invention is different. An implementation alternative according to the present clamed invention describes one of a plurality of possible alternatives to implement a specific circuit function in different alternative way as described on page 2, line 14 to 32 of the present application. According to the present invention, one of a plurality of parallel implementation alternatives is selected. This is not disclosed in Jain.

Furthermore Jain does not disclose that an implementation alternative with the greatest degree of structural equivalence with the digital circuit is determined and chosen form the plurality of parallel implementation alternatives to replace the description to the individual circuit structures in the reference description. Thus, the present invention of claim 1 compares and evaluates different implementation alternatives. Jain does not disclose such a comparison, evaluation or determination of implementation alternatives.

Next, the present invention of claim 1 teaches that specific circuit structures that are described by the reference description and that are a

portion of the reference description are replaced by the best fitting implementation alternative. In contrast, Jain teaches that an original specification is replaced by a circuit description as a whole if the complete description is found equivalent to the original to the original specification. Jain does not suggest replacing specific structures or parts of the complete circuit.

Furthermore, Jain is directed to a filter oriented approach to verification (Abstract, column 5, line 9). This means that the original specification is replaced by a qualified and filtered description that is checked for equivalence in order to avoid repeating verifications steps that have already been made. In contrast, the present invention of claim 1 is not related to any filtering of the description but to determining and finding out the most useful of a plurality of implementation alternatives that is used for the description of the digital circuit. Thus, the present invention as claimed differs substantially from Jain.

Finally, Jain discloses performing an equivalence test of a circuit description with respect to an original specification or a modified specification of the digital circuit. In contrast, the present invention claimed in claim 1 recited the step of executing an equivalence test by comparing the digital circuit itself with the reference description or modified reference description. This is also not disclosed or suggested in Jain.

Therefore, the present claimed invention of claim 1 differs in several substantial features from Jain. Consequently, the present invention is neither anticipated nor suggested by Jain and thus patentable over Jain. As claim 1 is patentable, dependant claims 2 to 13 and corresponding claims 14 to 17 are patentable as well.

Conclusion

In view of the above amendments and remarks, it is respectfully submitted that the present form of the claims are patentably distinguishable over the art of record and that this application is now in condition for allowance. Such action is requested.

Respectfully submitted,

June 17 2008
Date

John A. Lingl (Reg. No. 57,414)

Attachments: Replacement Sheet of the Drawing